Automated Testing of Mixed-Signal Integrated Circuits by Topology Modification

Anthony Coyette[1], Baris Esen[1], Ronny Vanhooren[2], Wim Dobbelaere[2] and Georges Gielen[1]

[1] Department of Electrical Engineering, KU Leuven,
Kasteelpark Arenberg 10, 3001 Leuven, Belgium
{anthony.coyette, georges.gielen, baris.esen}@esat.kuleuven.be

[2] ON Semiconductor Belgium,
{ronny.vanhooren, wim.dobbelaere}@onsemi.com

***Abstract*—A general method is proposed to automatically generate a DfT solution aiming at the detection of catastrophic faults in analog and mixed-signal integrated circuits. The approach consists in modifying the topology of the circuit by pulling up (down) nodes and then probing differentiating node voltages. The method generates a set of optimal hardware implementations addressing the multi-objective problem such that the fault coverage is maximized and the silicon overhead is minimized. The new method was applied to a real-case industrial circuit, demonstrating a nearly 100 percent coverage at the expense of an area increase of about 5 percent.**

Keywords*—Design-for-Testability, controllability, observability, low-overhead, co-optimization.

I. Introduction

The electronic world is evolving towards systems with a higher complexity and with increasing quantities of integrated circuits (ICs). For example, automotive chips are built into systems that contain hundreds of other electronic components and chips. As a consequence, the probability of a failing system increases due to the multiplication of the different defectivities. Also, applications such as the bio-medical or aerospacial ones require critical quality of the chips. In both cases a demand emerges and becomes stronger to acquire test techniques allowing to reduce and assess the defect level in the shipped products.

Research in digital ICs testing has led to defect level reaching the part per billion (ppb) range thanks to different advancements. First of all, the functional tests aiming at verifying the circuit performances and functionality were replaced by structural tests. These techniques focus on alternative features helping to match structurally the circuit under test with its design without considering the functionality. Next, progress was made by developing the concepts of controllability and observability. Algorithms such as PODEM [1] combining the two aspects form the basis of the efficient way to test digital ICs in the present industry.

In parallel, research on the testing of analog and mixed-signal ICs has tried to reiterate the digital success. Controllability has been studied in many perspectives. In [2] circuits are considered as black-boxes. The stimuli set is composed of sine waves resulting as the solution of a search problem. By including a generic insight about analog circuits [3] proposes to ramp up the power supply of the circuits under test to make some faults observable. In [4], specific information about the circuit under test is exploited thanks to the development of Testability Transfer Factors (TTF) to find stimuli maximizing the fault coverage. Finally, as for the digital case, controllability can be improved by Design-for-Testability (DfT) circuitry. In [5] a Built-in-Self-Test (BIST) technique creates a feedback system in order to make the circuit oscillate.

Similarly, observability offered by the outputs of the circuits has first been exploited [6]. Thanks to DfT, access to the internal nodes was gained and optimized. The choice of the optimal node voltage set, referred as test point selection, has been studied for electronic circuits in works such as [7] [8]. Non-intrusive techniques have been developed to enhance the observability as in [9].

However, a generic solution should result from a co-optimization combining observability and controllability in a flexible way. This has been presented in [10] [11]. In the same way as for digital testing, scan-chains have been added to observe node voltage and inject signals at specific nodes. But these solutions suffer from the need to open the signal path which is a practice considered as a bad practice among analog designers. Furthermore the problem of the signal to be injected in the circuit stays unsolved. [12] uses current branches and does not require the opening of signal paths. However, like the other scan-chain techniques previously cited, it suffers from a relatively high hardware overhead.

In this paper, a new generic method is introduced to enhance the controllability and the observability of mixed-signal circuits. Simple DfT building blocks with small hardware overhead are added and combined to improve the fault coverage. The main idea is to reconfigure the architecture of the circuit instead of injecting signal on nodes. This technique does not require the opening of the signal path. First, an overview of the fault-oriented methodology used to assess the efficiency of the method is addressed in Section II. Then, a general method enhancing the controllability and the observability of mixed-signal circuits is outlined in Section III. Afterwards, a possible hardware implementation is given in Section IV. Results for

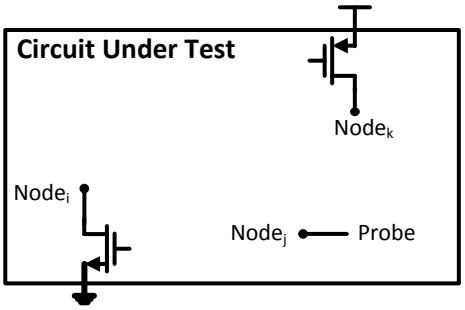


Fig. 1. Building blocks of the method.

an industrial case study demonstrate the effectiveness of the method in Section V. Finally, conclusions are drawn in Section VI.

II. Fault-Oriented Testing

Given an analog or mixed-signal circuit C_0, the defect-oriented methodology proposes to model the possible defects occurring at the transistor level and simulate them [13]. The flow starts with the generation of a list of the physical defects likely to appear in the manufactured chips. In the scope of this work, the faults modelling the defects are based on the schematic, but it could also start from the layout. In general, defects are categorized as catastrophic or parametric. The former emerges from a problem in the manufacturing process such as a dust particle or an over-etching. This causes a definitive change in the circuit i.e. shorts and opens. The latter results from the imperfect control of the process-voltage-temperature (PVT) conditions which may lead to tolerances causing certain devices to shift outside their specification range.

The present work focuses on applications using well mastered technologies (above 100nm) where parametric defects can be neglected to first order. Therefore, only catastrophic defects are studied. Furthermore, since the test circuit illustrating the presented method in Section V is designed in a technology using BJTs and MOSFETs, two different fault models often encountered in literature [14] are implemented. The fault model for the BJTs is a 6-fault model assuming that a short can happen between any pair of its three terminals and each terminal can be open. The model for the MOSFETs is a 5-fault model making the same assumptions as the 6-fault one. However the open gate fault is excluded because of the absence of an appropriate model for the DC simulations on which the presented technique is based. In both cases, the values of 100Ω and 1TΩ are used for modelling the short and open circuits respectively.

Based on the list of faults $L = \{F_1, ...F_D\}$, a list of possible faulty circuits is created. The assumption is made that two defects cannot occur in the same circuit. Hence, each fault is injected separately in the original circuit to create a faulty circuit. A circuit possessing D possible defects leads then to a set of D+1 circuits, i.e. the original circuit and the D faulty ones. Each of these D+1 circuits is simulated in SPICE in the presence of process variations. Signatures are extracted to distinguish the faulty cases from the good case. These signatures can be as simple as the measurement of the current consumption or of a node voltage. It is also possible to use signatures such as a Fast-Fourier-Transform or more sophisticated scheme based on measured transient signals [15].

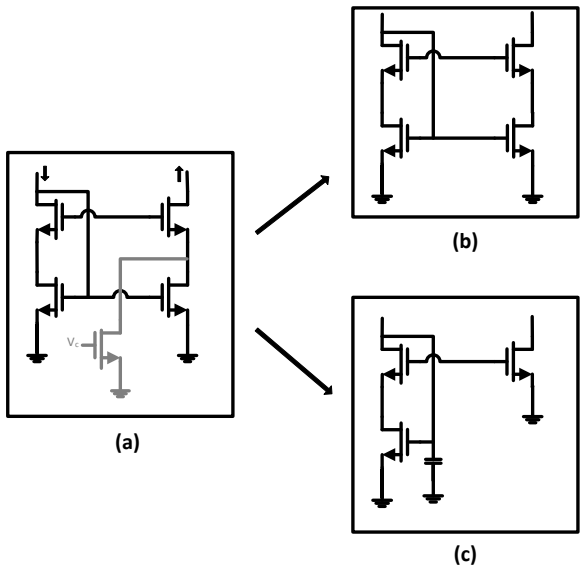


Fig. 2. Illustration of a topology modification:
(a) Current mirror with a Pull Down transistor.
(b) Topology in normal mode (V_c=0) : C_0.
(c) Topology in test mode (V_c=VDD) : C_1.

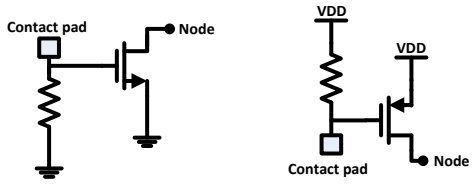
In the scope of this work, the exploited signatures are node voltages coming from DC simulations in the presence of process variations. Therefore, each of the D+1 circuits delivers a distribution which is assumed to be gaussian and represents the span of possible values for the voltage on the considered node. To assess the fault coverage, the signature of each of the D faulty circuits is compared to the signature of the original circuit. A fault F_i is considered as covered if its distribution $\mathcal{N}(\mu_{F_i}, \sigma_{F_i})$ is distant from the fault-free distribution $\mathcal{N}(\mu_G, \sigma_G)$ by at least 10mV and 3σ, where $\sigma = max(\sigma_G, \sigma_{F_i})$.

III. Test Scheme

As in the case of digital testing, and already applied in [10], the main idea is to enhance the controllability and observability simultaneously in a co-optimization. DC voltages are probed from internal nodes and primary output while the circuit is forced into different topologies. This technique distinguishes itself from existing schemes using the control offered by the circuit inputs or the internal injection of a signal by opening the signal path. The stimuli come from the modification of the circuit topology thanks to small and generic building blocks.

Instead of having a set of waveform as search space to optimize the fault coverage, the problem is transformed into a search for new topologies activating faults which were unobservable in the original circuit. Nevertheless, it is worth noting that the inclusion of the circuit inputs in the optimization system would lead to even more efficient solutions in terms of hardware overhead. This point will be illustrated in the study case of Section V.

The concept is first explained in details and a test procedure is proposed. Then, the method is expressed as an optimization



(a) PD transistor. (b) PU transistor.

Fig. 3. Control of PXs at the wafer level.

system to solve. Finally, possible improvements on the method are presented.

A. Topology Modification Approach

As introduced before, topology modifications are introduced into the circuit. These modifications aim at transforming the original circuit C_0 into new circuits having different behaviors. By operating this reconfiguration faults which were undetectable are made observable. This observability is based on the probing of voltages. While generally, for integrated circuits, only the input and output signals are assumed to be accessible [16], the internal nodes are supposed to be measurable through extra probes in the scope of this work. This hypothesis is supported by the hardware implementation proposed in Section IV and other works such as [17].

In summary, the test procedure can be summarized to a set of topologies $C_1, ..., C_k$ for which sets of circuits nodes are assigned $S_1, .., S_k$. Testing the circuit consists in applying each topology modification C_i, probe the corresponding set of nodes S_i and test these measurements against the corresponding decision threshold Th_i.

In this paper, topology modifications are realized by connecting nodes to the ground or the power supply. This is made possible by adding pull-down (PD) or pull-up (PU) transistors as illustrated in Figure 1. In the following, when the distinction between PD and PU is not essential, the discussion will be generalized by the use of the terminology PX to designate either a PD or a PU.

Figure 2 gives an illustration of the topology modification mechanism on a current mirror. The circuit originally consists of 4 transistors which are represented in black in Figure 2 (a). The gray nMOS transistor is a PD transistor that will operate the topology modification during the test mode. In normal mode the voltage imposed on the gate of this transistor is grounded. With a V_{GS} of 0V the transistor is in its cut-off region and the circuit C_0 is a normal current mirror as illustrated in Figure 2(b). In order to test the circuit, a set of node voltages S_0 is first measured in the original circuit. These values are compared to the ones expected from the simulations. Then, the PD transistor is activated such that the circuit topology changes to become the circuit C_1 seen in Figure 2(c). Another set of node voltages S_1 is measured and compared to the values expected from the simulations.

B. Optimization problem

In order to apply the proposed test procedure, the set of nodes to control (i.e. pull up or down) and the sets of node voltages to measure for each topology has to be calculated. These sets come as the solution of the optimization system developed in the following.

Given a circuit C_0, its set of internal nodes is labeled by T. The selection of nodes to control is operated on the sub-set N $\subset$ T. This pre-selection is done due to the large number of nodes present in industrial designs. In this work, the pre-selected nodes are the ones surrounding the transistors of the tested circuit with the exception of the digital gates. Other criteria can be added to refine or extend this pre-selection step. For instance, nodes that are extremely sensitive to parasitics can be excluded from the search set.

Each node contained in N leads to two possible topology modifications : one where the node is pulled up and one where the node is pulled down. This makes that $2\|T\| + 1$ circuits are finally considered i.e. the $2\|T\|$ topology variations and the original circuit, where $\|T\|$ designates the cardinality of the set T. For each of these, the fault-free and the D faulty circuits are simulated in the presence of process variations.

The second step after the simulations is to identify for each of the $2\|T\| + 1$ topologies which nodes allow to discriminate the good circuit from the faulty circuits. As said in Section II, for a topology C_i and a node $n \in N$, the fault F_i is considered detected if the distribution of simulated voltage for the good circuit and the faulty circuit are separated by at least 10mV or 3σ. The final results of these simulations is summarized in $2\|T\| + 1$ fault coverage vectors. Each vector contains D boolean values indicating for each fault if it is detected or not.

The third step consists in selecting which topologies should be used and which nodes should be probed. The problem of test points selection has already been addressed and solved in many works such as [7] [8]. More specifically, a co-optimization of the input stimuli and the selection of test points is formulated in [18]. However, instead of posing the optimization problem as a maximization of the fault coverage or a minimization of the tests set as it is usually done, the problem is set as a multi-objective optimization :

$$\underset{\substack{m \in \mathcal{P}(N) \\ p \in \mathcal{P}(T)}}{max} [FC_{co}(m,p), -\|p\|, -\|m\|]$$

where $FC_{co}(m,p)$ is a function computing the fault coverage when the nodes contained in m are controlled and the ones in p are probed with the output signals and $\mathcal{P}(X)$ designates the power set of X i.e. the set containing all the subsets of X. The present formulation is expressed in terms of size of node sets in its mathematical terms. However, once the building blocks are defined and designed as it is done in the next section, the optimization systems can be expressed in terms of silicon area.

This two-objective function aiming at maximizing the fault coverage and minimizing the silicon overhead is solved for the study case in the next section using a genetic algorithm described in literature as NSGA-II [19]. This tool is well suited for managing the search of Pareto optimal solutions in big search spaces.

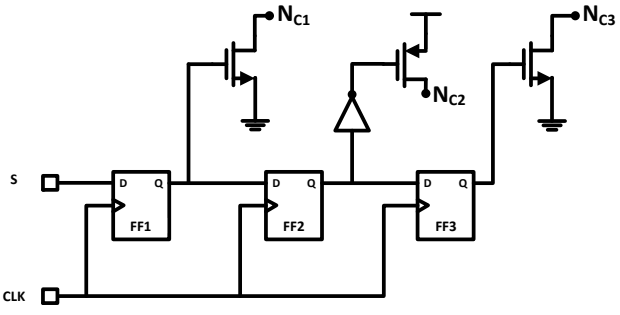


Fig. 4. A daisy-chain of flip-flops controlling the PXs.

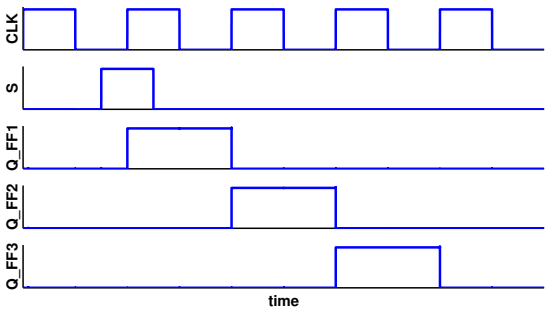


Fig. 5. Transient signals in the daisy-chain of Figure 4.

C. Extension

This technique forms a basis which can be further improved in controllability and observability. First, for the controllability, it should be noted that the PD and PU transistors are actually a particular case of topology modification. A more general approach consisting in connecting two nodes together could also be used at the expense of a rising computational complexity. This has not been studied in the scope of this paper, but it should be highlighted that this idea can also be seen as a generalization of the oscillation-based methods such as [5]. Indeed, these methods induce a feedback in a circuit in order to make them oscillate and a feedback connection is a particular case of the connection of two nodes. Furthermore, it is also worth noticing that the PXs are individually used. A finer optimization consisting in using several PXs in combination could lead to better results. However the complexity of such a method increases as the factorial of the number of nodes.

For the observability, this paper focuses on the probing of node voltages but other approaches can be used to improve the performances. Current monitoring systems were already studied in [20] and applied in control and observation structure (COS) in [12].

Finally, the method is presented for a set of DC measurements, but it should be noted that the same method can be exploited for transient signals. If a ramp is applied on the gate of a PX transistor the transition between the two topologies can be measured on an internal node. However, even if the question of dealing with transient signals can be addressed in a theoretical form, the hardware implementation rises technical issues.

IV. Proposed VLSI Implementations

In the previous section the basic building blocks and optimization method were explained. In this section practical solutions are presented to control the PX transistors and observe the selected node voltages. The basic hardware solutions which are proposed intend to demonstrate the feasibility and rely on existing work [10] [17]. These blocks can be enhanced to fulfill the resolution required by the applied detection mechanism.

It is worth noting that even though the case study developed in the next section is designed for a BCD technology, the proposed building blocks consists only of MOSFETs. This choice was taken due to the omnipresence of the CMOS technology and the aim of obtaining a technique tackling a large panel of different technologies.

A. Controlling

Industrial systems have a rapidly increasing complexity and are commonly composed of multiple sub-circuits organized hierarchically. Results have shown that a few PXs are required for each sub-circuit. The issue of controlling these elements independently rises rapidly since one pin cannot be assigned to each of them.

1) Wafer-Level Test: At wafer level, the routing of the signals controlling the gates of the PXs can be kept very small by introducing contact pads inside the circuit perimeter as illustrated in Figure 3. In the case of a PD transistor, the gate can be connected to GND through a resistor. Thanks to the contact pad connected to the gate an automated test equipment (ATE) can control directly the transistor. In normal mode, the voltage applied on the gate is the ground. With a V_{GS} equal to 0V the PD transistor is in its cut-off region and does not affect the circuit. When the wafer is under test, the ATE can impose a voltage on the gate. This allows the transistor to go into its active region and the desired topology modification takes place.

2) Packaged Device Test: In the case of a production test taking place on packaged dies, no direct access can be granted by contact pads. The controlling signal has to be routed from outside the ICs through a pin. In order to minimize the routing needed, a solution already used in digital and analog scan-chain [10] is proposed and illustrated in Figure 4.

In this approach only two interconnect lines are needed : one for the clock signal CLK and one for the control signal S. A daisy-chain of flip-flops can scan the control signal and the PX transistors can be activated successively. This mechanism is illustrated in Figure 5.

B. Observing

As the proposed technique not only relies on output signals from the circuits but also exploits internal node voltages, circuitry has to be added to obtain the access.

1) Wafer-Level Test: At wafer level, since basic DC measurements are required, the ATE can directly probe the node voltages through a contact pad added during the design step.

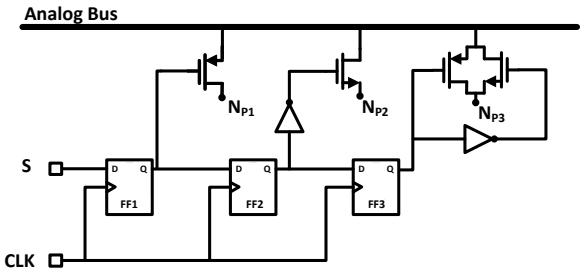


Fig. 6. A daisy-chain of flips-flops controls the pass gates.

Fault Coverage (percent)	Number of probes	Number of PXs
91.4	8	4
90.7	7	3
90	6	2
89.2	5	2
87.9	4	2
...	...	...
82.9	2	2
...	...	...
47.9	4	0
46.4	3	0
42.1	2	0
35	1	0
26.4	0	0

TABLE I. FIRST AND LAST 5 OPTIMAL SOLUTIONS IN THE PARETO FRONT.

2) Packaged Device Test: In the case of the packaged dies, the proposed solution for the probing of the internal nodes makes also use of daisy-chains scanning configuration bits in the DfT circuits. Figure 6 illustrates an example of a chain which involves the three possible configurations. A combination of these three different cases is needed because of the limited driving capacity of pMOS transistors when used as pass gates. A voltage in the range $[\text{VDD} - V_{th}; \text{VDD}]$ can not be transmitted since V_{GS} forces the transistor in its subthreshold region, where V_{th} is the threshold voltage of the transistor and VDD is the supply voltage of the circuit. The same limitation is encountered with nMOS transistors in the band $[0; V_{th}]$.

Therefore, if the set of DC voltages that have to be measured from a node of the circuit stays in the band $[0; \text{VDD} - V_{th}]$ (resp. $[V_{th}$;VDD]) a pMOS (resp. nMOS) is enough. In contrast, if the full range $[0; \text{VDD}]$ is required for a node, a full transmission gate is required to connect the node to the analog bus.

V. EXPERIMENTAL RESULTS

The proposed method has been applied to an industrial mixed-signal circuit designed using the 0.35μm I3T50 BCD technology provided by ON Semiconductor. Figure 7 shows the schematic of the Power-On-Reset (POR) circuit which will serve as case study. This circuit consists of an analog part and a digital part, containing in total 4 BJTs and 30 MOSFETs. This circuit possess one primary output and no primary input. It is an essential building block which keeps the chip in power-down mode as long as the voltage supply is too low. It is recognized as a hard-to-test circuit because of the Schmitt trigger it contains. Furthermore, faults on transistors like the 3 pMOS connected to the Power Saving Mode signal (PSM) are difficult to detect because they do not participate to the function of the POR.

First, the fault models introduced in Section II were applied on the schematic to generate a full list of the possible faults. The redundant cases (i.e. two different faults leading to the same simulation) were then removed and the test scheme proposed in Section III was carried out for the circuit with a list of 140 faults.

Table I shows the 5 first and the 5 last entries from the set of Pareto optimal solutions for the problem. An example of a hardware implementation is illustrated in Figure 7. The proposed hardware DfT is added in gray and allows to detect 116 faults with 2 PXs, 2 internal probes and 1 output probe.

Among the set of optimal solutions, two extremes can be found and show the importance of the controllability/observability co-optimization. The first extreme is the case where no PX is used. This observe-only solution covers 69 faults at the price of 5 probes, which is twice less than the 128 faults covered by the highest-coverage solution offered in the set of optimal solutions. This improvement demonstrates the limitations of an observability-only and the added value brought by the topology modification. The second extreme is the case where only PXs are used while the output signal is observed. In this case, 37 faults are covered proving the importance of enhancing the observability. To conclude, the three cases presented above show the importance to simultaneously enhance and co-optimize the controllability and observability of the tested circuits.

The analysis of the 12 remaining uncovered faults reveals that 10 of them are located in the digital gates at the end of the circuit. The lack of coverage for these gates emerges from the insufficient control on the digital input signals A and B. This results from the exclusion of the digital nodes and can be fixed by including the nodes of the digital gates in the set of usable nodes. This has not been done in this work since it is believed that the optimal solution should come from the combination of this method and a path sensitization technique such as typically used in digital test techniques.

Finally, the overhead created in terms of silicon area can be estimated. If the case where 128 faults are detected is considered, Table I indicates that 4 PXs are required. If it is chosen to implement this at package level, the proposed solution is largely dominated by the area of the flip-flop since the transistors for the pass gates and PXs are minimal size. Based on industrial designs, it can be estimated that the implementation of this solution would require an increase in silicon area of about 5 percent for the example POR circuit.

VI. CONCLUSION

A structured and automated method has been presented to address the problem of detecting faults in analog and mixed-signal integrated circuits. This was done in a generic way by replacing the traditional problem of finding a set of input

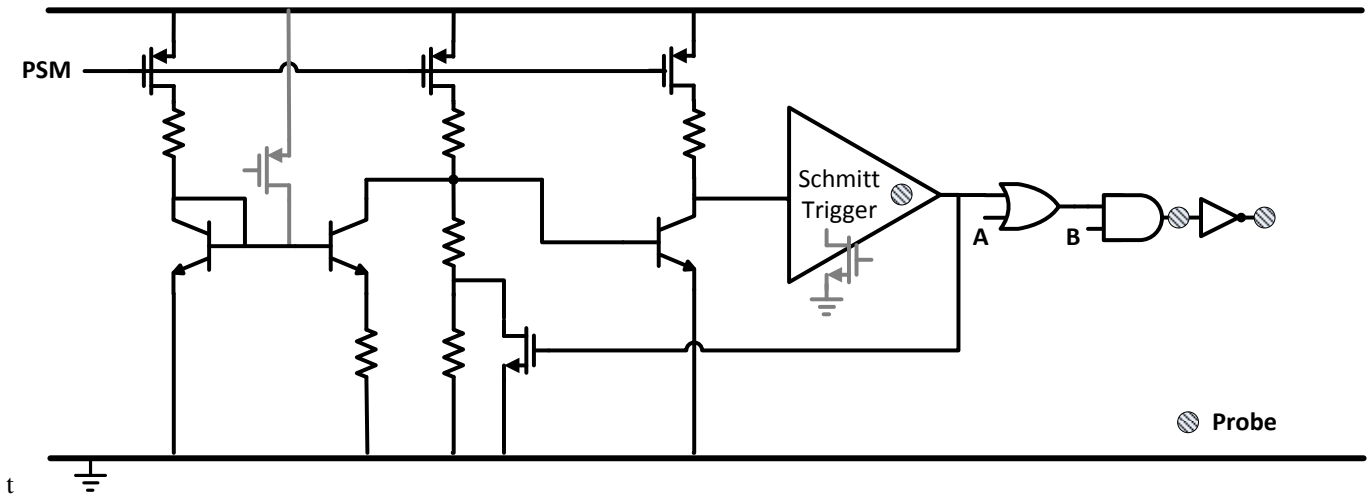


Fig. 7. Schematic of the Power-On-Reset with extra DfT blocks indicated.

signals allowing to control a circuit and make its faults detectable. Instead, a simple set of DC measurements combined to different circuit topology modifications are required. With different topologies, different faults are made observable.

Low-overhead hardware implementations were presented at wafer and package-levels. These allow to make the circuit under test adopt successively different topologies and probe DC node voltages during the test mode. Based on these building blocks, it was showed for an industrial Power-On-Reset circuit that nearly all the faults can be detected at the expense of around 5 percent of area overhead.

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